Amendment to the Claims

1. (Cancelled)

2. (Currently Amended) The system of claim ~~1~~ 25 wherein the first stori~~ng~~ age means (265) comprise a free buffer list (370) to allocate a free packet buffer location ~~(ID)~~ to each received data packet (360).

3. (Cancelled)

4. (Cancelled)

5. (Currently Amended) The system of claim ~~4~~ 25 wherein the number of source-priority registers and associated valid-bit latches ~~is~~ are equal to the number of ~~pairs of ingress adapters and~~ sources providing packets multiply by number of priority levels.

6. (Currently Amended) The system of claim ~~4 or~~ 5 wherein each of the plurality of source-priority registers further comprise counting means ~~(WPC)~~ to count for each sequence of data packets the number of data packets stored within said storing means waiting for being output from ~~the~~ at least one egress adapter.

7. (Currently Amended) The system of claims ~~1 or 2~~ 6 further comprising scheduling means (280) coupled to the ~~determination means~~ CAM and the

plurality of source priority registers for selecting one sequence of data packets from which a data packet is to be output from the at least one egress adapter.

8. (Original) The system of claim 7 wherein the scheduling means are coupled to the plurality of valid-bit latches to select one valid-bit latch among the valid-bit latches having their valid bit active.

9. (Currently Amended) The system of claims ~~1 or 2~~ 25 wherein the received data packets comprise unicast and multicast data packets.

10. (Currently Amended) The system of claim 9 wherein each of ~~the~~ a plurality of ingress adapters comprises means (210) for numbering the unicast data packets according to the priority level and to the at least one egress adapter of each unicast data packet.

11. (Original) The system of claim 10 wherein each of the plurality of ingress adapters further comprises means (205) for load balancing over a plurality of independent switching planes the numbered data packets.

12. (Original) The system of claim 11 wherein each of the plurality of ingress adapters further comprises means (220) for scheduling the switching of the unicast and multicast data packets over the plurality of independent switching planes.

13. (Currently Amended) The system of claim ~~7~~ 12 ~~wherein the~~ further including at least one egress adapter further comprises means (275) for numbering ~~the~~ multicast data packets according to the priority level of each multicast data packet and to ~~the~~ an independent switching plane each multicast data packet has been switched through.

14. (Currently Amended) A method for resequencing received data packets comprising for each received data packet:

~~a)~~ allocating a packet buffer location to the received data packet and temporarily storing said received data packet at said allocated packet buffer location;

~~extracting~~ using ~~the~~ a source identifier and ~~the~~ a priority level of the stored data packet to point to a corresponding source-priority register that contains a packet sequence number (PSN) and a packet buffer location identifier (ID) of a previously received data packet, the source-priority register being associated to a valid-bit latch that indicates an active / or not active status; ~~and~~

checking the status of the valid-bit latch; and
comparing the packet sequence number of the received data packet with the packet sequence number contained within the pointed source-priority register to determine if the received data packet is to be output as the next data packet of the corresponding sequence of data packets.

15. (Original) The method of claim 14 wherein the checking step (510) further

comprises:

(512) if the status is not active:

(518) updating the pointed source-priority register with the packet sequence number and the packet buffer location identifier of the received data packet, only if the packet sequence number of the received data packet is the next in sequence; and

setting the status of the valid-bit latch to active; otherwise,

(514) if the status is active:

(524) writing in a Content Addressable Memory, the source identifier, the priority level and the packet sequence number of the received data packet, the write address being identified by the packet buffer location allocated to the received data packet.

16. (Original) The method of claim 14 ~~or 15~~ further comprising incrementing a 'waiting packet' counter.

17. (Currently Amended) The method of claims 14 or 15 further comprising ~~the (600)~~ scheduling the output of the received data packet from ~~the~~ at least one egress adapter.

18. (Original) The method of claim 17 further comprising the step (602) of decrementing the 'waiting packet' counter after transmitting the received data packet.

19. (Currently Amended) The method of claim ~~17 or~~ 18 further comprising:

(604) searching the Content Addressable Memory for the next packet sequence number; and

(606) if the search match:

updating (608) the source-priority register with the founded next packet sequence number and the corresponding packet buffer location identifier;

keeping the status of the valid-bit latch to active; and

(610) invalidating the searched CAM entry; otherwise,

(612) if the search does not match, resetting (614) the status of the valid-bit ~~lacth~~ latch of the pointed source-priority register.

20. (Original) The method of claim 19 further comprising after the resetting starting a timer.

21. (Currently Amended) A system comprising:

a buffer in which received data packets are temporarily stored;

a controller programmed to use ~~the~~ a source identifier and ~~the~~ a priority level of the stored data packet to select a corresponding source-priority register that contains a packet sequence number (PSN) and a packet buffer location identifier (ID) of a previously received data packet, the source-priority register being associated with a valid-bit latch that indicates

an active ~~/~~ or not active status; and

said controller programmed to check the status of the valid-bit latch and comparing the packet sequence number of the received data packet with the packet sequence number contained within the pointed source-priority register to determine if the received data packet is to be output as the next data packet in the corresponding sequence of data packets.

22. (Currently Amended) A computer program product comprising:

a computer readable medium containing computer readable code including a first instruction module for accessing a buffer in which received data packets are temporarily stored and to ~~extract~~ use ~~the~~ a source identifier and ~~the~~ a priority level of the stored data packet to select a corresponding source-priority register that contains a packet sequence number (PSN) and a packet buffer location identifier (ID) of a previously received data packet, the source-priority register being associated to a valid-bit latch that indicates an active ~~/~~ or not active status; and

a second instruction module to check the status of the valid-bit latch and comparing the packet sequence number of the received data packet with the packet sequence number contained within the pointed source-priority register to determine if the received data packet is to be output as the next data packet of the corresponding sequence of data packets.

23. (Currently Amended) A method comprising:

a) providing a buffer in which packets exiting a device is temporarily stored;

b) providing at least one source priority register identifying at least one packet by at least Source , Priority (S_1, $P_{1\text{-}n}$), Packet ~~Serial~~ Sequence No. (PSN) and location of packet in said buffer ~~(ID)~~;

c) providing at least one validity latch whose setting indicates status of said at least one packet; and

d) scheduling a packet for transmission based upon state of the validity latch.

24. (Currently Amended) The method of claim 23 including repeating d) so long as another packet having a packet ~~serial~~ sequence number in-sequence with a last scheduled packet is found in the buffer.

25. (Newly Added) A system for resequencing received data packets comprising:

a first means for storing each received data packet at an allocated location within said first means;

a Content Address Memory (CAM) having at least one entry comprising an identification field to contain a packet buffer identifier (ID) field to identify an allocated location in said first means whereat a received data packet is placed, a search field to contain a source identifier of a source providing said receive data packet, a priority level for said receive data packet and a sequence number for said receive data packet, wherein recited fields are concatenated;

a plurality of source-priority registers each containing, a packet sequence number (PSN) and a packet buffer identifier (ID) of a data packet previously transmitted from said first means; and

a plurality of valid-bit latches respectively associated to the plurality of source-priority registers to set an active status to indicate that corresponding stored data packet is the next one in sequence.